SiMOS Quantum Dot Spin Qubits

Our group has driven the development of spin qubits based on Silicon-Metal-Oxide-Semiconductor (SiMOS) quantum dots, which we first developed in 2007 [1]. Since that time we have demonstrated a wide range of SiMOS quantum dot devices and have developed both 1-qubit and 2-qubit logic gates based on this technology. These SiMOS quantum dots have also been crucial to single-P-atom spin qubit readout and control.

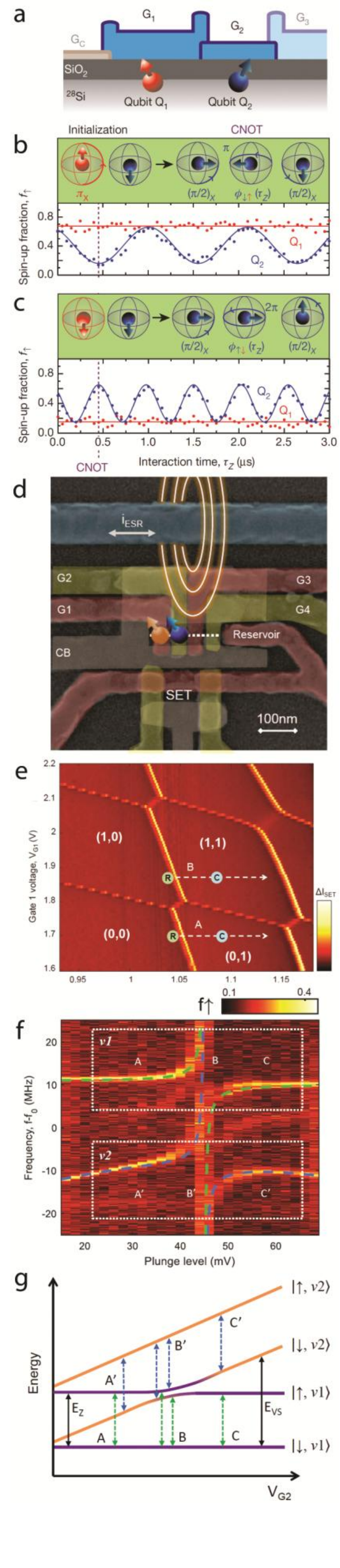
Quantum dot qubits require a large energy splitting between the Si conduction band valleys. In 2013 we demonstrated that the valley separation can be tuned over a large range via electrostatic gate control in our Si-MOS quantum dots [2]. The splitting varies strongly with applied electric field. In 2016, in a collaboration with Sandia National Laboratory, a detailed theoretical analysis showed excellent agreement with experimental gate-controlled valley splitting in devices fabricated at both Sandia and UNSW [3].

By integrating a Si-MOS quantum dot with an on-chip microwave line we can operate the device as an **electron spin qubit** [4]. When fabricated using ^{28}Si, the dephasing time T_2^* = 120 μs is the longest observed for any quantum dot qubit, leading to a high control fidelity F_C = 99.6%.

In 2015 we published in *Nature* the first demonstration of a **two-qubit logic gate in silicon** [5], based on two exchange-coupled SiMOS quantum dot qubits – see Figure a-c. We realize CNOT gates via controlled-phase operations combined with single-qubit operations (via ESR). Direct gate-voltage g-factor control provides single-qubit addressability, while a gate voltage switchable exchange interaction is used for the two-qubit controlled-phase gate (Figure b).

These SiMOS qubits have excellent prospects for scaling to large numbers of qubits and in 2016 we developed designs for both 1D and 2D qubit arrays. In a collaboration with researchers at HRL Laboratories (USA) we showed that our quantum dot qubits could be configured in a 1D array to realize a logical qubit, with a fault-tolerant error threshold of order 10^{-4} [6]. Looking further into the future, we also developed a detailed design for a quantum processor chip based on a 2D array of quantum dots [7] that could be manufactured using CMOS manufacturing. We showed that our 2D architecture [7] could employ surface code based error correction, making possible much higher error tolerance ~10^{-2}. While beyond the scope of this Centre, these results provide a pathway for longer-term developments of large-scale quantum computing.

In 2016 we further investigated the important role of valley states in spin-based qubits by using ESR as a sensitivity probe of the valley physics. Our PhD student Jason Hwang, with Dr Henry Yang, used ESR on a single-electron qubit to map out the anti-crossing which occurs when the Zeeman energy (spin splitting) equals the valley splitting – see Figure f,g [8]. They also showed that a two-qubit gate could be realised using only ESR pulses in a double-dot system when the exchange coupling is comparable to the g-factor difference ($\Delta g \mu_B B$) between the dots [8].



One- and two-qubit gates using SiMOS quantum dot spin qubits.
(a) Schematic depicting two electron spin qubits Q_1 and Q_2 confined under gates G_1 and G_2. **(b,c)** Spin-up fraction of both qubits after initializing Q_1 spin up (b) and spin down (c) using a microwave pulse and applying a controlled rotation (via exchange) using Q_2 as the target qubit. A CNOT gate is achieved in 480 ns. (a-c) taken from Ref. [5] **(d)** SEM image of a multi-dot device for the study of 1- and 2-qubit gates. **(e)** Charge stability map of a double dot system confined under gates G1 and G2. **(f)** ESR spectrum of a single qubit operated in the (1,1) charge region in (e). **(g)** Energy level schematic showing the crossing of spin and valley states, with marked spin transitions corresponding with ESR spectra in (f). (d-g) taken from Ref. [8].

References

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